In the Claims

1. (presently amended) A method used to etch a conductive layer to result in a selected profile of the conductive layer, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer;

forming a conductive layer over the semiconductor wafer, wherein the conductive layer comprises first and second vertically-oriented cross-sectional sidewalls, each sidewall comprising a lower portion and an upper portion continuous with the lower portion, with the upper portion being further away from the wafer than the lower portion;

selecting a post-etch profile from first, second, and third post-etch profiles, wherein:

the first post-etch profile results from an etch which removes lower and upper portions of each sidewall of the conductive layer at about the same rate to result in a substantially vertical profile of the conductive layer;

the second post-etch profile results from an etch which removes the lower portion of each sidewall of the conductive layer at a faster rate than it removes the upper portion to result in a substantially U-shaped profile of the conductive layer; and

the third post-etch profile results from an etch which removes the lower portion of each sidewall of the conductive layer at a faster rate than it removes the upper portion to result in the conductive layer having a profile which tapers inward at a uniform rate from the upper sidewall portion to the lower sidewall portion; ~~and~~ then

etching the conductive layer using an etch comprising a flow rate of between about 6 sccm and about 12 sccm ~~HeO_2~~ $He\text{-}O_2$ to result in the conductive layer having the selected post-etch profile,

wherein the ~~HeO_2~~ $He\text{-}O_2$ flow rate is about 6 sccm to result in the conductive layer having the first profile;

wherein the ~~HeO_2~~ $He\text{-}O_2$ flow rate is about 9 sccm to result in the conductive layer having the second profile; and

wherein the ~~HeO_2~~ $He\text{-}O_2$ flow rate is about 12 sccm to result in the conductive layer having the third profile.

2. (presently amended) The method of claim 1 wherein the etch of the conductive layer further comprises:

a flow rate of 50 sccm HBr;

a flow rate of an additional 100 sccm He;

a ~~lower~~ bias power of 70 watts;

~~an upper~~ a TCP power of 350 watts ~~upper~~; and

a pressure of 60 mTorr.

3. (original) The method of claim 1 further comprising forming a polysilicon layer during the formation of the conductive layer.

4. (presently amended) A method used during the formation of a semiconductor device, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer;

forming a blanket conductive layer over the semiconductor wafer;

forming a silicide layer on the conductive layer;

forming a dielectric layer on the silicide layer;

etching the dielectric layer, the silicide layer, and the blanket conductive layer to form first and second sidewalls,

wherein each sidewall is defined by the conductive layer, the silicide layer, and the dielectric layer, and

wherein a lower portion of the conductive layer is closer to the semiconductor wafer than an upper portion of the conductive layer;

selecting a post-etch profile from first, second, and third post-etch profiles, wherein:

the first post-etch profile results from an etch which removes lower and upper portions of the conductive layer at about the same rate to result in a substantially vertical profile of the conductive layer;

the second post-etch profile results from an etch which removes the lower portion of the conductive layer at a faster rate than it removes the upper portion of the conductive layer to result in a substantially U-shaped profile of the conductive layer; and

the third post-etch profile results from an etch which removes the lower portion of the conductive layer at a faster rate than it removes the upper portion of the conductive layer to result in the conductive layer having a profile which tapers inward at a uniform rate from the upper sidewall portion to the lower sidewall portion; ~~and~~ then

with the silicide layer on the conductive layer and the dielectric layer on the silicide layer, etching the conductive layer using an etch comprising a flow rate of between about 6 sccm and about 12 sccm ~~HeO_2~~ $He\text{-}O_2$ to result in the conductive layer having the selected post-etch profile,

wherein the ~~HeO_2~~ $He\text{-}O_2$ flow rate is about 6 sccm to result in the conductive layer having the first profile;

wherein the ~~HeO_2~~ $He\text{-}O_2$ flow rate is about 9 sccm to result in the conductive layer having the second profile; and

wherein the ~~HeO_2~~ $He\text{-}O_2$ flow rate is about 12 sccm to result in the conductive layer having the third profile.

5. (presently amended) The method of claim 4 wherein the etch of the conductive layer further comprises:

a flow rate of 50 sccm HBr;

a flow rate of an additional 100 sccm He;

a ~~lower~~ bias power of 70 watts;

~~an upper~~ a TCP power of 350 watts ~~upper~~; and

a pressure of 60 mTorr.

6. (original) The method of claim 1 wherein the conductive layer is polysilicon.

7. (original) The method of claim 6 wherein the dielectric layer is nitride.